Operational Semantics of a Weak Memory Model with Channel Communication

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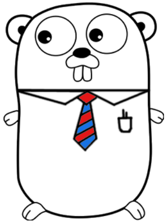
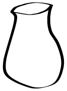
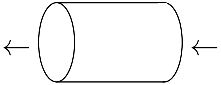




memory
model



channel
communication

$$\frac{\bullet \Rightarrow \blacksquare \quad \bullet}{\blacksquare}$$

operational
semantics

What’s a memory model?

A memory model dictates what values can be read from memory at a given point in the execution

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- In a single thread case $\Rightarrow$ program order
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Initially $\mathtt{z} = 0$

```
      T0               |       T1
z    := 42             |
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$\mathtt{z} = 42$

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$\texttt{z} = 42$ $\qquad$ $\texttt{flag} = 1 \;\Rightarrow\; \texttt{z} = ?$

Sequential consistency

Memory as a shared global repository where operations appear atomic and in program order

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$z = 42$ $\qquad\qquad$ $flag = 1 \Rightarrow z = 42$

Sequential consistency

Memory as a shared global repository where operations appear atomic and in program order

+ Simple to reason bout
- Does not reflect modern hardware
- Restricts compiler optimizations

Initially $\mathtt{z} = 0$

```
     T0               |        T1
z    := 42            |
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$\mathtt{z} = 42$ $\qquad\qquad$ $\mathtt{flag} = 1 \;\Rightarrow\; \mathtt{z} = 42$

Weak memory

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     T0            |        T1
z    := 42         |
flag := 1          |    load flag
load z             |    load z
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$\texttt{z} = 42$ $\texttt{flag} = 1 \;\Rightarrow\; \texttt{z} \in \{0, 42\}$

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We took inspiration from the Go language

Models often described from a hardware-centric perspective

- Write buffers, caches, (pipeline) flushes, etc.

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- focus on reasoning about program behavior
- account for hardware and compiler implementations
- but not concerned with being “implementable”

  Freed us to think about a (potentially) simpler model

- *Within a single thread,*
    - *reads and writes must behave as if they executed in the order specified by the program;*

replace *thread* by *goroutine*
[Go memory model, 2014]

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Order and Observability

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A relation on events. $e \rightarrow_{\mathsf{hb}} e'$

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z     := 42   (A)            |    load flag   (C)
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- Just because $\texttt{A} \rightarrow_{\text{hb}} \texttt{B}$, it does not mean `A` occurred before `B`
- Just because `B` occurred before `C`, it does not mean $\texttt{B} \rightarrow_{\text{hb}} \texttt{C}$

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       T0                |       T1
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- Just because $\mathtt{A} \rightarrow_{\mathsf{hb}} \mathtt{B}$, it does not mean `A` occurred before `B`
- Just because `B` occurred before `C`, it does not mean $\mathtt{B} \rightarrow_{\mathsf{hb}} \mathtt{C}$

No ordering between events of different threads

$$\mathtt{A} \rightarrow_{\mathsf{hb}} \mathtt{B} \wedge \mathtt{C} \rightarrow_{\mathsf{hb}} \mathtt{D} \quad \not\Rightarrow \quad \mathtt{A} \rightarrow_{\mathsf{hb}} \mathtt{D}$$

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A read r of variable z can observe a write w also to z **unless**:

- $r \rightarrow_{\text{hb}} w$
- $w \rightarrow_{\text{hb}} w' \rightarrow_{\text{hb}} r$
  for some write w' to z

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```
  T'
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z := 2
load z
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   T'
z := 1   (A')
z := 2   (B')
load z   (C')
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$\mathtt{A'} \rightarrow_{\text{hb}} \mathtt{B'} \rightarrow_{\text{hb}} \mathtt{C'}$

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`A` $\rightarrow_{\mathrm{hb}}$ `B`

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`A'` $\rightarrow_{\mathrm{hb}}$ `B'` $\rightarrow_{\mathrm{hb}}$ `C'`

`B'` shadows `A'`

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relative to a thread

Our model

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When a thread reads from memory:

- read any write event that is not in its *shadowed set*

When a thread writes to memory it update its local state:

- recording the write as having happened in the past
- recording writes that became un-observable

$$\frac{}{p\langle \sigma, \texttt{let}\ r = \texttt{load}\ z\ \texttt{in}\ t\rangle}\ \textsc{Read}$$

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$$\frac{\sigma = (\_, E_s) \qquad m \notin E_s}{\begin{array}{c} p\langle \sigma, \texttt{let}\ r = \texttt{load}\ z\ \texttt{in}\ t\rangle \parallel m(\!|z{:=}v|\!) \\ \Rightarrow \quad p\langle \sigma, \texttt{let}\ r = v\ \texttt{in}\ t\rangle \parallel m(\!|z{:=}v|\!) \end{array}}\ \textsc{Read}$$

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$$\frac{\mathit{fresh}(m)}{p\langle\sigma, z := v; t\rangle \quad\Rightarrow\quad p\langle\sigma', t\rangle \parallel m\llparenthesis z{:=}v\rrparenthesis}\ \textsc{Write}$$

$$\dfrac{\sigma = (E_{hb}, E_s) \qquad\qquad \mathit{fresh}(m)}{p\langle \sigma, z := v; t\rangle \quad \Rightarrow \quad p\langle \sigma', t\rangle \parallel m(\!|z{:=}v|\!)}\ \textsc{Write}$$

$$\frac{\sigma = (E_{hb}, E_s) \qquad \sigma' = (E_{hb} + (m, z), E_s + E_{hb}(z)) \qquad \mathit{fresh}(m)}{p\langle \sigma, z := v; t\rangle \quad \Rightarrow \quad p\langle \sigma', t\rangle \parallel m(\!| z{:=}v |\!)}\ \textsc{Write}$$

Synchronization

Motivating example

```
  Producer             |      Consumer
z    := 42   (A)       |  while (flag != 1) {}     (C)
flag := 1    (B)       |  load z                   (D)
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Synchronization via channel communication

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Synchronization via channel communication

```
  Producer             |      Consumer
z    := 42   (A)       |  while (flag != 1) {}     (C)
c    <- 0    (B)       |  load z                   (D)
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Synchronization via channel communication

$A \rightarrow_{\mathsf{hb}} D$

$$\frac{}{p\langle \sigma, c \leftarrow v; t\rangle \quad \| \; c[q]}\;\textsc{Send}$$

$$\frac{}{\begin{array}{ll} p\langle \sigma, c \leftarrow v; t\rangle & \parallel c[q] \quad \Rightarrow \\ p\langle \sigma', t\rangle & \parallel c[(v, \sigma) :: q] \end{array}} \textsc{Send}$$

$$\frac{\neg closed(c[q_2]) \qquad \sigma' = \sigma + \sigma''}{\begin{array}{rcl} c_b[q_1 :: \sigma''] \parallel & p\langle \sigma, c \leftarrow v; t\rangle & \parallel c[q_2] \quad \Rightarrow \\ c_b[q_1] \parallel & p\langle \sigma', t\rangle & \parallel c[(v, \sigma) :: q_2] \end{array}} \textsc{Send}$$

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$$\frac{v \neq \bot \qquad \sigma' = \sigma + \sigma''}{\begin{array}{r}c_b[q_1] \parallel \quad p\langle \sigma, \texttt{let } r = \leftarrow c \texttt{ in } t\rangle \quad \parallel c[q_2 :: (v, \sigma'')] \quad \Rightarrow \\ c_b[\sigma :: q_1] \parallel \quad p\langle \sigma', \texttt{let } r = v \texttt{ in } t\rangle \quad \parallel c[q_2] \qquad\qquad\end{array}}\ \textsc{Rec}$$

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    - is *thread local*
    - and travels on channels, implicitly

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- Order (HB) and observability (shadowing)
  - is *thread local*
  - and travels on channels, implicitly

Synchronization as restriction on observability

Correctness

Relating the weak model to a sequentially consistent model

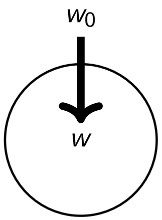
P

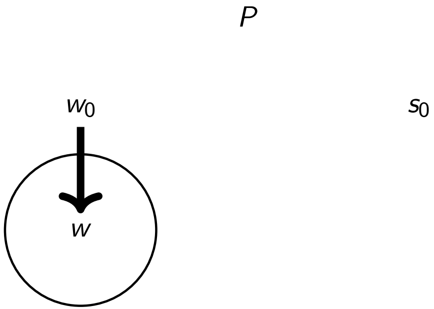
P

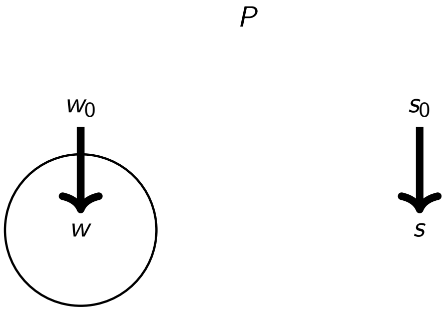
w_0

$$\begin{tikzcd} & P \\ w_0 \arrow[d] & \\ w & \end{tikzcd}$$

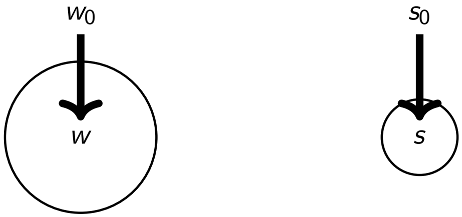
P



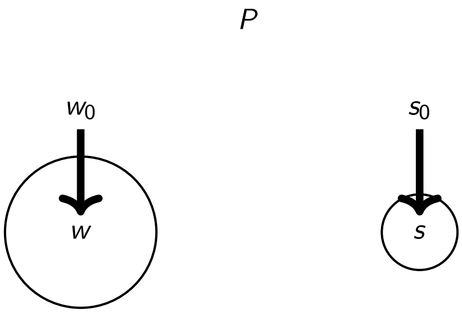

P
w_0
s_0
w


P
w_0
w
s_0
s

P

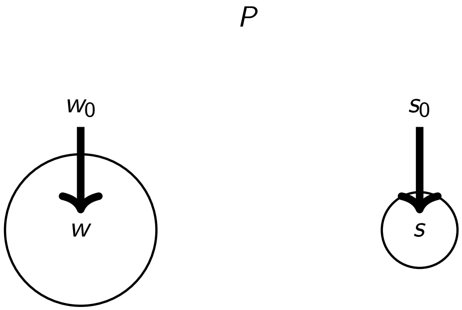


A property desired of weak memory models



A property desired of weak memory models

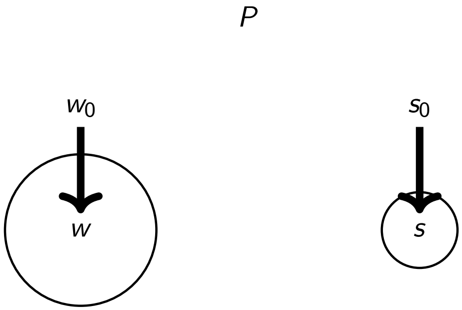
Sequentially consistent data-race free (SC-DRF) guarantee



A property desired of weak memory models

Sequentially consistent data-race free (SC-DRF) guarantee

- Allows programmers to think in terms of strong memory
- Write it once, run it everywhere
    - provided program is DRF and memory models are SC-DRF



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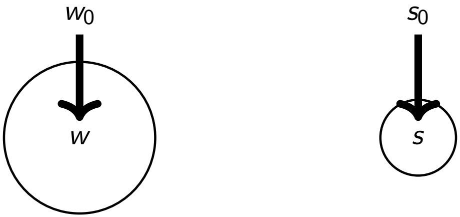
$DRF(P)$



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$DRF(P)$

We prove a desired property of the model

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Proof of conditional simulation

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$$DRF(P)$$

$$\begin{tikzcd} w_0 \arrow[r, dash] & \mathcal{R} \arrow[r, dash] & s_0 \end{tikzcd}$$

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$$DRF(P)$$

$$\begin{tikzcd} w_0 \arrow[r, dash] \arrow[d, "\alpha"'] & \mathcal{R} \arrow[r, dash] & s_0 \\ w & & \end{tikzcd}$$

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$DRF(P)$

$$\begin{tikzcd}
w_0 \arrow[r, dash, "\mathcal{R}" description] \arrow[d, "\alpha"'] & s_0 \arrow[d, dotted, "\alpha"'] \\
w & s
\end{tikzcd}$$

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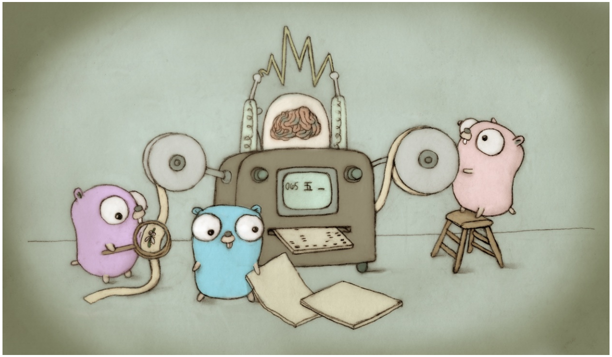
$$\begin{tikzcd}
w_0 \arrow[rr, dash, "\mathcal{R}" description] \arrow[d, "\alpha"'] & & s_0 \arrow[d, dotted, "\alpha"'] \\
w \arrow[rr, dash, dotted, "\mathcal{R}" description] & & s
\end{tikzcd}$$

We have implemented our semantics in $\mathbb{K}$, which is an executable semantics framework

Available on the mmGo GitHub page
`https://github.com/dfava/mmgo`

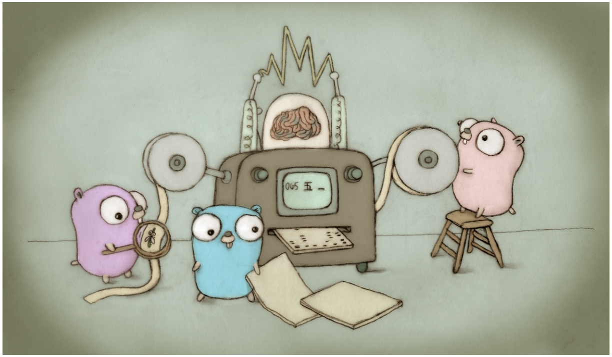
Hypothesis. We can use the semantics for data-race detection



Hypothesis. We can use the semantics for data-race detection

Current goal. To relax model by accounting for read buffers

i.e. branching on values read but not yet "resolved"



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Questions?

References

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