Ready, set, Go!

Data-race detection and the Go language

Daniel S. Fava danielsf@ifi.uio.no

Martin Steffen msteffen@ifi.uio.no



Department of informatics University of Oslo, Norway SBMF'19 São Paulo, Brazil

Data races

Data races

Subtle bugs

Data races

- ► Subtle bugs
- Unknown semantics (under weak-memory)

A memory model informs us how our multi-threaded programs behave.

A memory model informs us how our multi-threaded programs behave.

Initially z = 0; done = false; T1 | T2 z = 42 | done = true | while (!done) {} | print("t2", z) Relaxed memory models are complex.

If program is Data-Race Free (DRF) then memory behaves Sequentially Consistently (SC).

Ρ

Ρ

If program is Data-Race Free (DRF) then memory behaves Sequentially Consistently (SC).

Ρ

Ρ

If program is Data-Race Free (DRF) then memory behaves Sequentially Consistently (SC).

Ρ

If program is Data-Race Free (DRF) then memory behaves Sequentially Consistently (SC).

 $\llbracket P \rrbracket_w$







 \checkmark Race detection & message passing.

Race detection & message passing.

- ► No shared memory.
- ► Races as competing to send-to/receive-from channels.
- Absence of races imply determinism.

Race detection & message passing.

- ► No shared memory.
- ► Races as competing to send-to/receive-from channels.
- Absence of races imply determinism.

Origin of the happens-before relation and vector clocks.



Data-race detection & locks
Shared memory, but
no channels,
no synchronization via message passing.

We express race-detection for a language with message passing as the sole synchronization primitive.

We express race-detection for a language with message passing as the sole synchronization primitive.



We express race-detection for a language with message passing as the sole synchronization primitive.



II. Background

A *data race* constitutes memory accesses that *conflict* and are *concurrent*.

A *data race* constitutes memory accesses that *conflict* and are *concurrent*.

Conflict { same memory location, at least one access is a write. A *data race* constitutes memory accesses that *conflict* and are *concurrent*.

Conflict { same memory location, at least one access is a write.

Concurrent: not ordered by happens-before.

[Go memory model, 2014] replacing *thread* by *goroutine*

► Within a single thread,

 reads and writes must behave as if they executed in the order specified by the program;

> [Go memory model, 2014] replacing *thread* by *goroutine*

► Within a single thread,

- reads and writes must behave as if they executed in the order specified by the program;
- reorder is allowed only when it does not change the behavior within that thread.

[Go memory model, 2014] replacing *thread* by *goroutine*

- ► Within a single thread,
 - reads and writes must behave as if they executed in the order specified by the program;
 - reorder is allowed only when it does not change the behavior within that thread.
- The execution order observed by one thread may differ from the order observed by another.

[Go memory model, 2014] replacing *thread* by *goroutine*
Initially z = 0; done = false; T1 | T2 z = 42 | done = true | if (done) ______ | print("t2", z) Initially z = 0; done = false; T1 | T2 z = 42 (A) | done = true (B) | if (done) (C) | print("t2", z) (D)

 ${\tt A} \to_{\sf hb} {\tt B}$

T1 | T2 z = 42 (A) | done = true (B) | if (done) (C) | print("t2", z) (D)

 $A \rightarrow_{hb} B$ $C \rightarrow_{hb} D$

The Go memory model.

[Go memory model, 2014]

The Go memory model.

A send happens-before the corresponding receive completes.

[Go memory model, 2014]

The Go memory model.

A send happens-before the corresponding receive completes.

Given a channel *c* with capacity *k*, the *i*th receive from *c* happens-before the (i + k)th send completes.

[Go memory model, 2014]

$A \rightarrow_{hb} B$ ($\mathtt{C} \rightarrow_{ert}$	hb	D
--------------------------	--------------------------------	----	---



 $A \rightarrow_{hb} B \qquad \qquad C \rightarrow_{hb} D$





$$A \rightarrow_{hb} B$$
 $C \rightarrow_{hb} D$



$$A \rightarrow_{hb} B \qquad \qquad C \rightarrow_{hb} D$$



$$A \rightarrow_{hb} B \qquad \qquad C \rightarrow_{hb} D$$

$$A \rightarrow_{hb} B \qquad \qquad C \rightarrow_{hb} D$$

$$\begin{array}{ccc} A \rightarrow_{hb} B & & C \rightarrow_{hb} D \\ & & B \rightarrow_{hb} C \end{array}$$

$$\begin{array}{ccc} {}_{A \rightarrow_{hb} B} & & {}_{C \rightarrow_{hb} D} \\ & {}_{B \rightarrow_{hb} C} \end{array} \\ & A \longrightarrow_{hb} D \end{array}$$

III. Our approach

III. Our approach

Intuition

III. Our approach

Intuition

Efficiency

Each thread keeps track of events in its past

• Happened-before set, E_{hb}

Each thread keeps track of events in its past

• Happened-before set, E_{hb}

A memory cell keeps track of

- ► a variable's value
- set of events that have happened-before to the variable, E_{hb}

$p\langle E_{hb},t\rangle$

$$p\langle E_{hb}, t \rangle$$
 $(E_{hb}^z, z := v)$

$$p\langle E_{hb},t\rangle \parallel (E_{hb}^z,z:=v)$$

$$p\langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^z, z := v)$$

$$\begin{array}{l} p\langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', t \rangle \parallel (E_{hb}', z := v') \end{array}$$

$$\begin{array}{l} p\langle E_{hb}, z := v'; t\rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', t\rangle \parallel (E_{hb}'^z, z := v') \end{array}$$

fresh(m)

$$\begin{array}{l} p\langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', t \rangle \parallel (E_{hb}', z := v') \end{array}$$

(m, !z)

fresh(m)

 $\begin{array}{l} p\langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', t \rangle \parallel (E_{hb}', z := v') \end{array}$
fresh(m)
$$E'_{hb} = \{(m, !z)\} \cup E_{hb}$$

$$\begin{array}{l} p\langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', t \rangle \parallel (E_{hb}', z := v') \end{array}$$

$$fresh(m) \qquad \begin{array}{l} E_{hb}' = \{(m, !z)\} \cup E_{hb} \\ E_{hb}'^{z} = \{(m, !z)\} \cup E_{hb}^{z} \\ \hline p \langle E_{hb}, z := v'; t \rangle \parallel (E_{hb}^{z}, z := v) \\ \rightarrow p \langle E_{hb}', t \rangle \parallel (E_{hb}'^{z}, z := v') \end{array}$$

A write is allowed to proceed if...

$$fresh(m) \qquad \begin{array}{l} E'_{hb} = \{(m, !z)\} \cup E_{hb} \\ E'^z_{hb} = \{(m, !z)\} \cup E^z_{hb} \\ p\langle E_{hb}, z := v'; t \rangle \parallel (E^z_{hb}, z := v) \\ \rightarrow p\langle E'_{hb}, t \rangle \parallel (E'^z_{hb}, z := v') \end{array}$$

A write is allowed to proceed if...

$$fresh(m) \qquad \begin{array}{l} E'_{hb} = \{(m, !z)\} \cup E_{hb} \\ E'^z_{hb} = \{(m, !z)\} \cup E^z_{hb} \\ p\langle E_{hb}, z := v'; t \rangle \parallel (E^z_{hb}, z := v) \\ \rightarrow p\langle E'_{hb}, t \rangle \parallel (E^z_{hb}, z := v') \end{array}$$

$$p\langle E_{hb}, \text{let } r = \text{load } z \text{ in } t \rangle \parallel (E_{hb}^z, z := v)$$

$$p\langle E_{hb}, \text{let } r = \text{load } z \text{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow p\langle E_{hb}', \text{let } r = v \text{ in } t \rangle \parallel (E_{hb}^{'z}, z := v)$$

$\begin{array}{l} p\langle E_{hb}, \texttt{let } r = \texttt{load } \overline{z } \texttt{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', \texttt{let } r = v \texttt{ in } t \rangle \parallel (E_{hb}'^z, z := v) \end{array}$

fresh(m)

$$\begin{array}{l} p\langle E_{hb}, \texttt{let } r = \texttt{load } z \texttt{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', \texttt{let } r = v \texttt{ in } t \rangle \parallel (E_{hb}'^z, z := v) \end{array}$$

fresh(m)

$$\begin{array}{l} p\langle E_{hb}, \texttt{let } r = \texttt{load } z \texttt{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', \texttt{let } r = v \texttt{ in } t \rangle \parallel (E_{hb}'^z, z := v) \end{array}$$

fresh(m)
$$E'_{hb} = \{(m, ?z)\} \cup E_{hb}$$

$$\begin{array}{l} p\langle E_{hb}, \texttt{let } r = \texttt{load } z \texttt{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow \quad p\langle E_{hb}', \texttt{let } r = v \texttt{ in } t \rangle \parallel (E_{hb}'^z, z := v) \end{array}$$



A read is allowed to proceed if...

$$fresh(m) \begin{array}{c} E_{hb}' = \{(m,?z)\} \cup E_{hb} \\ E_{hb}'^z = \{(m,?z)\} \cup E_{hb}^z \\ \hline p \langle E_{hb}, \texttt{let } r = \texttt{load } z \texttt{ in } t \rangle \parallel (E_{hb}^z, z := v) \\ \rightarrow p \langle E_{hb}', \texttt{let } r = v \texttt{ in } t \rangle \parallel (E_{hb}', z := v) \end{array}$$

A read is allowed to proceed if...

$$\frac{fresh(m)}{p\langle E_{hb}, \text{let } r = \text{load } z \text{ in } t\rangle || (E_{hb}^z, z:=v)}{p\langle E_{hb}, \text{let } r = v \text{ in } t\rangle || (E_{hb}^z, z:=v)}$$

Sends and Receives transmit a thread's happens-before set

Sends and Receives transmit a thread's happens-before set Threads "learn" from each other about past events

Channel receive

$$\begin{array}{c|c} v \neq \bot & E_{hb}' = E_{hb} + E_{hb}'' \\ \hline c_b[q_1] \parallel & p \langle E_{hb}, \texttt{let} \ r = \leftarrow \ \texttt{c} \ \texttt{in} \ t \rangle & \parallel \ \texttt{c}_f[q_2 :: (v, E_{hb}'')] \ \rightarrow \\ c_b[E_{hb} :: q_1] \parallel & p \langle E_{hb}', \texttt{let} \ r = v \ \texttt{in} \ t \rangle & \parallel \ \texttt{c}_f[q_2] \end{array}$$

Channel receive

$$egin{aligned} & v
eq ot & E_{hb}' = E_{hb} + E_{hb}'' \ \hline c_b[q_1] \parallel & p \langle E_{hb}, \texttt{let} \ r = \leftarrow \ c \ \texttt{in} \ t
angle & \parallel c_f[q_2 :: (v, E_{hb}'')] &
ightarrow \ c_b[E_{hb} :: q_1] \parallel & p \langle E_{hb}', \texttt{let} \ r = v \ \texttt{in} \ t
angle & \parallel c_f[q_2] \end{aligned}$$

Channel receive

$$egin{aligned} & v
eq eta & E_{hb}' = E_{hb} + E_{hb}'' \ \hline & c_b[q_1] \parallel & p \langle E_{hb}, \texttt{let} \ r = \leftarrow \ c \ \texttt{in} \ t
angle & \parallel c_f[q_2 :: (v, E_{hb}'')] &
ightarrow \ c_b[E_{hb} :: q_1] \parallel & p \langle E_{hb}', \texttt{let} \ r = v \ \texttt{in} \ t
angle & \parallel c_f[q_2] \end{aligned}$$

Channel send



Efficiency



























$$(E_{hb}^z, z:=v)$$

$$(E_{hb}^{z}, z:=v)$$

 $(m, !z), (m', ?z) \in E_{hb}^{z}$
$$(E_{hb}^{z}, z:=v)$$

 $(m, !z), (m', ?z) \in E_{hb}^{z}$

$$(E_{hb}^{z}, z:=v)$$

 $(m, !z), (m', ?z) \in E_{hb}^{z}$

$$m(E_{hb}^r, z:=v)$$

$$(E_{hb}^{z}, z:=v)$$

 $(m, !z), (m', ?z) \in E_{hb}^{z}$

$$m(E_{hb}^r, z := v)$$

$$(E_{hb}^{z}, z:=v)$$

 $(m, !z), (m', ?z) \in E_{hb}^{z}$

 $m(E_{hb}^r, z := v)$ $E_{hb}^z \downarrow_! \qquad (m, !z)$





























Updated *write*-rule for efficient race detection.

$$(m, !z) \in E_{hb} \qquad E_{hb}^r \subseteq E_{hb} \qquad \text{fresh}(m')$$
$$E_{hb}' = \{(m', !z)\} \cup (E_{hb} - E_{hb} \downarrow_z)$$
$$p\langle E_{hb}, z := v'; t\rangle \qquad \parallel m(E_{hb}^r, z := v) \rightarrow p\langle E_{hb}', t\rangle \qquad \parallel m'(\emptyset, z := v')$$

Updated *read*-rule for efficient race detection.

$$\begin{array}{ll} (m, !z) \in E_{hb} & fresh(m') \\ E_{hb}^{\prime r} = \{(m', ?z)\} \cup (E_{hb}^{\prime} - E_{hb} \downarrow_z) \\ E_{hb}^{\prime} = \{(m', ?z)\} \cup (E_{hb} - E_{hb} \downarrow_z) \cup \{(m, !z)\} \\ p \langle E_{hb}, \text{let } r = \text{load } z \text{ in } t \rangle & \parallel m(E_{hb}^{\prime}, z := v) \rightarrow \\ p \langle E_{hb}^{\prime}, \text{let } r = v \text{ in } t \rangle & \parallel m(E_{hb}^{\prime r}, z := v) \end{array}$$

Offline garbage-collection.

$$\begin{split} E_{hb}' &= E_{hb} \quad - \{ (\hat{m}, |z) \mid (\hat{m}, |z) \in E_{hb} \land \hat{m} \neq m \} \\ &- \{ (\hat{m}, ?z) \mid (\hat{m}, ?z) \in E_{hb} \land (\hat{m}, ?z) \notin E_{hb}' \} \end{split}$$
$$p \langle E_{hb}, t \rangle \parallel m(E_{hb}', z := v) \rightarrow p \langle E_{hb}', t \rangle \parallel m(E_{hb}', z := v)$$

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

In Djit⁺ and FastTrack, each thread u has a vector clock C_u ,

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

In Djit⁺ and FastTrack, each thread u has a vector clock C_u , where it keeps:

► its own time,

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

In Djit⁺ and FastTrack, each thread u has a vector clock C_u , where it keeps:

- ► its own time,
- the time of the most recent operation by v known to u.

Vector clocks, Djit,⁺ and FastTrack.⁺

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

In Djit⁺ and FastTrack, each thread u has a vector clock C_u , where it keeps:

- ► its own time,
- the time of the most recent operation by v known to u.

C_u

Vector clocks, Djit,⁺ and FastTrack.⁺

Think of a clock as natural number. A *vector clock* maps a thread id to a clock.

In Djit⁺ and FastTrack, each thread u has a vector clock C_u , where it keeps:

- ► its own time,
- the time of the most recent operation by v known to u.

 $C_u(v)$

Memory per thread

Djit⁺ FastTrack

Our approach

Memory per thread

Djit⁺ FastTrack Our approach $O(\nu\tau)$

 $O(\tau)$ worst-case

 τ number of threads ν number of variables

au number of threads

 ν number of variables

 $\begin{array}{c} \mathsf{Djit}^+\\ \mathsf{Memory\ per\ thread} & \mathsf{FastTrack} & \mathsf{Our\ approach}\\ \mathsf{worst-case} & \mathcal{O}(\tau) & \mathcal{O}(\nu\tau)\\ \mathsf{best-case} & \mathcal{O}(1) & \mathcal{O}(1) \end{array}$

au number of threads u number of variables

Comparison with TSan.

Also in the paper

Rules for

- synchronous communication
- dynamic channel and thread creation
- ► data-race reporting, etc

Connection with trace theory





Data-race detection in terms of channel communication


Data-race detection in terms of channel communication

message passing as synchronization primitive



Data-race detection in terms of channel communication

- message passing as synchronization primitive
- ► no vector-clocks; based directly on happens-before relation

Summary

Data-race detection in terms of channel communication

- message passing as synchronization primitive
- ► no vector-clocks; based directly on happens-before relation
- most recent write, most recent reads, garbage collection

Summary

Data-race detection in terms of channel communication

- message passing as synchronization primitive
- ► no vector-clocks; based directly on happens-before relation
- most recent write, most recent reads, garbage collection
- ► models happens-before as described by the Go memory model

► Implementation

- ► Implementation
- Proof of "minimality of information"

- Implementation
- Proof of "minimality of information"

Least amount of event information that must be kept Largest amount of information that can be garbage collected

- Implementation
- Proof of "minimality of information"

Least amount of event information that must be kept Largest amount of information that can be garbage collected

- Implementation
- Proof of "minimality of information"

Least amount of event information that must be kept Largest amount of information that can be garbage collected

Questions?

References

- Go memory model (2014). The Go memory model. https://golang.org/ref/mem.
 Version of May 31, 2014, covering Go version 1.9.1
- Fava, D. and Steffen, M. (2019). Ready, set, Go! Data-race detection and the Go language. To appear in the pre-proceedings of the Brazilian Symposium on Formal Methods (SBMF). http://arxiv.org/abs/1910.12643

References

- Fava, D., Steffen, M., and Stolz, V. (2018b). Operational semantics of a weak memory model with channel synchronization.
 Journal of Logic and Algebraic Methods in Programming.
 An extended version of the FM'18 publication with the same title
- Fava, D., Steffen, M., and Stolz, V. (2018a). Operational semantics of a weak memory model with channel synchronization.

In Havelund, K., Peleska, J., Roscoe, B., and de Vink, E., editors, *FM*, volume 10951 of *Lecture Notes in Computer Science*, pages 1–19. Springer Verlag

 French, R. Gopher figure by Renee French. https://blog.golang.org/gopher